What is Claimed is:

1. A composite memory device, comprising:

a first asynchronous memory device;

a second synchronous memory device configured to operate in a page mode;

a third synchronous memory device configured to operate in a burst mode;

a memory bus configured to transfer data among the first through the third memory devices;

a first memory controller configured to control data transfer operation between the first memory device and the memory bus;

a second memory controller configured to control data transfer operation between the second memory device and the memory bus; and

a third memory controller configured to control data transfer operation between the third memory device and the memory bus,

wherein the first through the third memory devices are controlled by an external memory controller to exchange data with an external system bus, and

when one of the first through the third memory devices exchanges data with the external system bus, the

rest two memory devices are allowed to exchange data via the memory bus.

2. The device according to claim 1, further comprising a serial interface controller configured to control data transfer operation between the memory bus and an external serial system bus.

3. The device according to claim 1, further comprising:

a central processing unit;

a system bus configured to transfer data among the central processing unit and the first through the third memory devices; and

a memory controller configured to control data transfer operation between the system bus and a memory device among the first through the third memory devices and controlled by the central processing unit.

4. The device according to claim 3, further comprising:

a serial system bus configured to receive serial data; and

a serial interface controller configured to control

data transfer operation between the memory bus and the serial system bus.

5. The device according to claim 1, wherein the first memory device is a ferroelectric memory device.

6. The device according to claim 5, wherein the first memory device comprises:

a cell array block including a plurality of cells arranged as a matrix format, each cell connected to a wordline, a plateline and a bitline;

a driver configured to drive the wordline and the plateline in response to a row address decoder;

a column selection controller configured to connect a data bus to the bitline in response to a column address decoder;

a data I/O buffer connected to the system bus; and

a sense amplifier array configured to control data input/output operation between the data bus and the data I/O buffer in response to the column address decoder,

wherein the first memory controller is connected between the sense amplifier array and the memory bus and controls data exchange operation between the cell array block and the memory bus.

7. The device according to claim 1, wherein the second memory device is a ferroelectric memory device.

8. The device according to claim 7, wherein the second memory device comprises:

a cell array block including a plurality of cells arranged as a matrix format, each cell connected to a wordline, a plateline and a bitline;

a driver configured to drive the wordline and the plateline in response to a row address decoder;

a column selection controller configured to connect a data bus to the bitline in response to a column address decoder;

a data I/O buffer connected to the system bus; and

a sense amplifier array configured to control data input/output operation between the data bus and the data I/O buffer in response to the column address decoder,

wherein the second memory controller is connected between the sense amplifier array and the memory bus and controls data exchange operation between the cell array block and the memory bus.

9. The device according to claim 1, wherein the

third memory device is a ferroelectric memory device.

10. The device according to claim 9, wherein the third memory device comprises:

a cell array block including a plurality of cells arranged as a matrix format, each cell connected to a wordline, a plateline and a bitline;

a burst counter configured to receive a column address from a column address buffer and to control a column address decoder so that the column address may increase consecutively;

a driver configured to drive the wordline and the plateline in response to the column address decoder;

a column selection controller configured to connect a data bus to the bitline in response to the column address decoder;

a data I/O buffer connected to the system bus; and

a sense amplifier array configured to control data input/output operation between the data bus and the data I/O buffer in response to the column address decoder,

wherein the third memory controller is connected between the sense amplifier array and the memory bus and controls data exchange operation between the cell array block and the memory bus.

11. The device according to claim 1, wherein the first through the third memory devices are a ferroelectric memory device.

12. The device according to claim 1, wherein the first through the third memory devices are MRAMs (Magnetic Random Access Memory).

13. The device according to claim 1, wherein the first through the third memory devices are PRAMs (Phase Change Random Access Memory).

14. The device according to claim 1, wherein the second memory device is a flash memory device.

15. A composite memory device, comprising:

a plurality of memory devices configured to operate individually;

a memory bus configured to transfer data among the plurality of memory devices; and

a plurality of memory controllers configured to control data transfer operation between the memory bus and a memory device among the plurality of the memory devices

respectively,

wherein the plurality of memory devices are controlled by an external memory controller to exchange data with an external system bus, and

when one of the plurality of memory devices exchanges data with the external system bus, the rest memory devices are allowed to exchange data via the memory bus.